UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,559	09/22/2000	Noboru Matsuda	197226US-2TTC	9685

22850 7590 01/15/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
FARAHANI, DANA

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/667,559	MATSUDA ET AL.	
	Examiner	Art Unit	
	Dana Farahani	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 3, 4, 6, 7, 9, 11, 13-15, and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu (U.S. 4,663,644), previously cited.

Regarding claim 3, the device in figure 10 comprises a first gate electrode group (middle electrodes) having a plurality of gate electrodes 23 formed on a semiconductor substrate to be away from each other at first equal spacings; a source contact portion 32 formed separated from the first gate electrode group to be away from the first gate electrode groups at a second spacing; and source regions 27 for electrically interconnecting the first gate electrode group and the source contact, wherein the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group.

Regarding claim 4, the semiconductor device in figure 10 comprises a first gate electrode group between other two groups having a plurality of gate electrodes 23 formed on a semiconductor substrate to be away from each other at first equal spacings; a second gate electrode group at the right hand side of the first group having a plurality of gate electrodes 23 formed on the semiconductor substrate to be away from each other at the first equal spacings: a source contact portion 32 between the first and

second gate electrode groups to be away from the first and second gate electrode groups at a second spacing; and source regions 27 for electrically interconnecting the first gate electrode group and the source contact, wherein the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group.

Regarding claim 6, the gate electrode groups are formed in trench structures.

Regarding claim 7, each of the source regions is a diffused layer formed on the semiconductor substrate.

Regarding claim 9, there is a source electrode 33 on the semiconductor substrate, wherein the source contact portion is an electrode drawn from the source electrode.

Regarding claims 11 and 13, the semiconductor device in figure 10 comprises a first gate electrode group, between the other two groups, having a plurality of gate electrodes 23 formed on a semiconductor substrate to be away from each other at first equal spacing; a second gate electrode group to the right of the first group having a plurality of gate electrodes 23 on the semiconductor substrate to be away from each other at the first equal spacing; a third gate electrode group to the left of the first group having a plurality of gate electrodes 23 formed on the substrate to be away from each other at the first equal spacing; a first source contact portion 32 formed between the first and second gate electrode groups to be away from the first and second gate electrode groups at a second spacing; a second source contact portion 32 formed between the second and third gate electrode groups to be away from one selected from the second

and third gate electrode groups at the second spacing; first source regions 27 which electrically interconnect the first gate electrode group and the first source contact portion; and second source regions which electrically interconnect the second gate electrode group and the second source contact, wherein the first source regions are connected to each other at one end of the first gate electrode group and are separated from each other at the other end of the first gate electrode group, and the second source regions are connected to each other at one end of the second gate electrode group and are separated from each other at the other end of the second gate electrode group.

Regarding claim 14, the first and second gate electrode groups are formed in trench structures.

Regarding claim 15, each of the first and second source regions is a diffused layer formed on the semiconductor substrate.

Regarding claim 17, each of the first andsecond source contact portions is an electrode drawn from a source electrode 33, and these portions are connected to each other.

Regarding claim 18, all the gate electrodes of the first and second gate electrode groups are used as gates for MOS transistors.

Regarding claim 19, the second source regions are connected to each other at one end of the second gate electrode group, and separated from each other at the other end of the second gate electrode group.

Regarding claim 20, the second spacing is greater than the first spacing.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 8, 10, 12, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu in view of Bergemont et al., hereinafter Bergemont (U.S. Patent 5,889,700), newly cited.

Shimizu discloses the claimed invention, as discussed above, except for the gates in the group being connected to each other, and the gates of the groups being connected to each other, also.

Bergemont discloses at column 2, lines 39-51, that gates of transistor elements in a memory array is connected to a common word line. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect all the gates to each other in order to be able to use the transistor structure of Shimizu in a memory array.

Response to Arguments

5. Applicant's arguments filed on 11/4/02 have been fully considered but they are not persuasive.

Applicants primarily argue that "Shimizu does not disclose or suggest that the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group" as claim 4 recites. Claim 4 recites, among other things, "...source regions for electrically interconnecting the first gate electrode group and the source contact, wherein the source regions are connected to each other at one end of the first gate electrode group, and separated from each other at the other end of the first gate electrode group." As can be seen in figure 10 of Shimizu, there are source regions 27, which connect, via electrode 33, the first and second gate electrode groups (the group in the middle of the three gate electrode groups shown in the figure, and the group to its right, respectively); and wherein the source regions are connected to each other at one end of the first gate electrode group (that is at the right hand end of the first gate electrode group), and separated from each other at the other end (left) of the gate electrode group. Note that the source regions are connected via 33.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
January 8, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800